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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,996	12/15/2003	G. Glenn Henry	CNTR.2152	2970

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EXAMINER	
FIEGLE, RYAN PAUL	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,996	HENRY ET AL.	
	Examiner	Art Unit	
	Ryan P. Fiegle	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 February 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1-29 are objected to because the use of "micro instruction." The common use is to compound the words as "microinstruction." Though correction is not required, doing so will make a patent, if issued, more easily searchable and hence more easily enforceable.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 6-9 and 16-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims recite "each..." but don't say each what. For the purposes of this action, based on the specification and the corresponding method claims, the examiner has guessed that the applicant meant to say "each micro instruction queue entry," for each instance.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4-6, 11, 12, 14-16, 21, 22, and 24-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Carbine et al. (US Patent 5,222,244).

3. As per claim 1:

A microprocessor apparatus, for precluding a pipeline stall due to microcode ROM access delay, the microprocessor apparatus comprising:

a plurality of micro instruction queue entries, each corresponding to an instruction, and said each comprising a plurality of micro instructions and a microcode entry point (column 6, lines 58-68; column 7, lines 1-19); and

early access logic, coupled to said micro instruction queue, configured to employ said microcode entry point to access a microcode ROM prior to when said microcode entry point is provided to register logic, whereby said microcode ROM provides a first micro instruction to said register logic when said first micro instruction is required by said register logic (column 8, lines 39-43).

4. As per claim 2:

The microprocessor apparatus as recited in claim 1, wherein said each of said plurality of micro instruction queue entries is provided in order to said register logic (column 6, lines 58-68; column 7, lines 1-19).

5. As per claim 4:

The microprocessor apparatus as recited in claim 1, wherein said plurality of micro instructions comprises three micro instructions (column 7, lines 8-11).

6. As per claim 5:

The microprocessor apparatus as recited in claim 4, wherein the microcode ROM access delay comprises four clock cycles (It is inherent that the delay is 4 cycles since the queue contains the first three instructions).

7. As per claim 6:

The microprocessor apparatus as recited in claim 1, wherein said early access logic employs said microcode entry point when said microcode entry point is within a bottom micro instruction queue entry, said bottom micro instruction queue entry comprising one of said each, and wherein said bottom micro instruction queue entry will be provided to said register logic during a next clock cycle (column 6, lines 58-68; column 7, lines 1-19; column 8, lines 39-43).

8. As per claim 11:

An apparatus for absorbing pipeline stalls associated with microcode ROM access delay, the apparatus comprising:

a micro instruction queue, for providing a plurality of queue entries to register logic, each of said plurality of queue entries comprising:

first micro instructions, all of said first micro instructions corresponding to an instruction; and

a microcode entry point, coupled to said first micro instructions, configured to point to second micro instructions stored within a microcode ROM (column 6, lines 58-68; column 7, lines 1-19); and

early access logic, coupled to said micro instruction queue, configured to employ said microcode entry point to access said microcode ROM prior to when said each of

said plurality of queue entries is provided to said register logic, whereby a first one of said second micro instructions is provided to said register logic when said first one of said second micro instructions is required by said register logic (column 8, lines 39-43).

9. As per claims 12 and 14-16:

Claims 12 and 14-16 recite the same limitations as claims 1, 2 and 4-6 and are rejected for the same reasons.

10. As per claims 21, 22 and 24-26:

Claims 21, 22 and 24-26 recite the method of the apparatus of claims 1, 2 and 4-6 with the same limitations and therefore are rejected for the same reasons.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 3, 13 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carbine et al. (US Patent 5,222,244).

13. As per claim 3:

Carbine does not teach his queue containing four micro instruction queue entries; however, such would have been obvious to one of ordinary skill in the art.

Four entries provides a simpler design with a lower latency than designs with a greater number of entries. Further, less than four entries would not be beneficial because there would not be enough entries to make the additional logic beneficial.

In addition, it has been found that changing the size of an element does not designate a patentable difference if the invention would operate in the same manner. In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

Therefore, it would have been obvious to one of ordinary skill in the pertinent art that providing four entries in Carbine would provide the benefits of a simple logic and low latency while still providing the overall benefits of the invention.

14. Claims 13 and 23 recite the same limitations as claim 3 and therefore are rejected for the same reasons.

15. Claims 7-10, 17-20 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carbine et al. (US Patent 5,222,244) in view of the background of the application.

16. As per claim 7:

Carbine et al. do not teach the microprocessor apparatus as recited in claim 1, further comprising:

a translator, coupled to said plurality of micro instruction queue entries, configured to generate said microcode instruction queue entry (column 6, lines 58-68; column 7, lines 1-19).

Carbine does not disclose how the contents of the queue entries are determined.

However, the applicant has disclosed as prior art that the combination of a microcode ROM and a direct translator for the sequencing of macroinstructions is known in the art.

The combination of the microcode ROM and a direct translator in coordination with the microcode queue would be a viable, beneficial solution in Carbine.

An opposing possibility would be to statically populate the queue with the most commonly used instructions. One of ordinary skill in the pertinent art would have recognized that this would not be extremely useful because it would only provide the benefits of not stalling on a microcode ROM instruction in the instance of encountering a common instruction, which might not extend across different applications.

In contrast, a queue that is dynamically populated by a translator when the microcode ROM instruction is first encountered will provide the benefits of the invention to all microcode ROM instructions.

Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that providing a translator to generate the microinstruction queue entries in Carbine would provide the benefit of not stalling on any microcode ROM instruction, rather than a select few.

As per claim 8:

The microprocessor apparatus as recited in claim 7, wherein said translator is configured to provide a generated micro instruction queue entry to a top micro instruction queue entry, wherein said top micro instruction queue entry comprises one of

said each micro instruction queue entry (This corresponds to the common LIFO definition of a queue).

17. As per claim 9:

The microprocessor apparatus as recited in claim 7, wherein said translator is configured to provide a generated micro instruction queue entry to a mux, and, when said plurality of micro instruction queue entries is empty, said mux provides said generated micro instruction queue entry to said register logic during a next clock cycle (It would have been obvious to one of ordinary skill in the pertinent art that if the queue is used in a LIFO manner where an entry is dequeued each cycle, an entry enqueued to an empty queue will take 5 cycles to reach the register logic which negates the purpose of the queue. Therefore, a bypass from the translator to the register logic would have been an obvious variation to one of ordinary skill in the pertinent art.).

18. As per claim 10:

The microprocessor apparatus as recited in claim 9, wherein said early access logic employs a bypass microcode entry point corresponding to said generated micro instruction queue entry (It is obvious that an entry point to the ROM will still need to be generated since the ROM will still need to be accessed after the first three instructions.).

19. Claims 17-20 and 27-29 recite the same limitations as claims 7-10 and are rejected for the same reasons.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

21. Carbine et al. (US Patent 6,378,061) also discloses Intel's microinstruction queue.

22. Shaw et al. (US Patent 5,870,553) discloses a similar method used for video-on-demand.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegle whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan P Fiegle
Examiner
Art Unit 2183

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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